ECUcore-iMX35

Hardware Manual

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Index of figures and tables

1 Introduction

This manual describes the function and technical data for the ECUcore-iMX35, but not for the microcontroller Freescale iMX35 or any other supplemental products. Please refer to the corresponding manuals and documentation for any other products you may use.

Low-active signals are denoted by a „/“ in front of the signal name (i.e. “/RD”). The representation “0” indicates a logical-zero or low-level signal. A “1” is the synonym for a logical one or high-level signal.

2 Ordering Information and Support

Order Number	Version
4001025	ECUcore-iMX35
4002018	Development Kit ECUcore-iMX35

The ECUcore-iMX35 features:

- High-performance CPU (ARM 32-Bit ARM1136JF-S, 532 MHz CPU Clock, 740 MIPS)
- 128 MiB DDR2 RAM Memory, 128 MiB FLASH Memory
- LCD Controller supports up to 800x600 pixel resolution with 24-bit color depth
- Support for Scrollwheel and 4x4 Matrix keypad
- 1x 10/100 Mbps Ethernet LAN interface (with on–board PHY)
- 2x CAN 2.0B interface, usable as CANopen Manager (CiA 302-conform)
- 3x asynchronous serial ports (UART)
- 16 digital inputs, 10 digital outputs (standard configuration, modifiable via DDK)
- Externally usable SPI and I^2C
- On-board peripherals: RTC, watchdog, power-fail input
- Single power supply 3,3V (all other voltages are derived on-board)
- ESD Handling Instructions (printed version)

3 Properties of the ECUcore-iMX35

3.1 Overview

The ECUcore-iMX35 belongs to SYS TEC's ECUcore family. The ECUcore-iMX35 combines all elements of a microcontroller system on one board. With the help of modern SMD packages and the multilayer design, the module was designed at minimum size.

Figure 1: ECUcore-iMX35

The dimensions of the board are 78mm x 54mm and it includes two board connectors which makes it multifunctional in embedded systems.

The ECUcore-iMX35 features a Freescale i.MX35 microcontroller. It is a highly-integrated 32-bit microprocessor based on the ARM1136JF-S architecture.

The interconnection to a customer board is possible through a pair of low-density (2mm pitch) connectors with 200 pins in total.

The ECUcore-iMX35 includes the following features:

- Internal features of the Freescale i.MX35:
    - Internal 532MHz CPU-clock from external 16MHz
    - 16kByte Data- / 16kByte instruction L1 cache, MMU
    - 128kByte L2 cache
    - 128kByte of internal SRAM
    - Vector floating point unit (VFP11)
    - Image processing unit (IPU)
    - OpenVG 1.1 2.5D hardware accelerator
    - 32-bit mobile DDR, DDR2 (4-bank architecture), and SDRAM (up to 133MHz)
    - 2 configurable serial peripheral interfaces (CSPI) (up to 52 Mbps each)
    - 2 synchronous serial interfaces (SSI)
    - USB2.0 full speed 1xOTG, 1x host
    - 1 Fast Ethernet controller MAC
    - Smart DMA controller with 32 channels
    - LCD controller (up to 24-bit, 800 x 600)
    - 3x USART
    - 2x Part 2.0A and Part 2.0B compliant CAN controller
    - 2 configurable serial peripheral interfaces (CSPI) (up to 52 Mbps each)
    - Flash controller—MLC/SLC NAND and NOR
    - 2 SDIO/MMC interfaces, 1 SDIO/CE-ATA interface
    - 3x I2C interface up to 400kbits
    - 2x 32bit Timer/Counter
    - JTAG/ICE interface
    - SPDIF transceiver

- Memory configuration:
    - up to 128MiByte NOR-Flash
    - up to 128MiByte DDR2 RAM
- Communication features:
    - 1 Ethernet interface
    - 3 UARTs as LVTTL
    - 2 CAN as LVTTL
    - 1 USB device full speed
    - 1 USB host full speed
    - 2 SPI with 4 chip select
    - I²C interface
- Other board-level features:
    - Ethernet PHY
    - Micro SD-Card slot
    - LVDS controller (optional)
    - Touch controller
    - Battery-buffered Real time clock
    - Temperature sensor
    - 32KiByte SPI EEPROM for data storage
    - JTAG/Embedded ICE interface
    - 24MHz crystal for PLL, 16MHz crystal for audio purposes
    - 3.3V operating voltage
      on-board generated voltage for CPU
    - Industrial temperature range (-40°C to +85°C)
    - RoHS compliant

3.2 Block Diagram

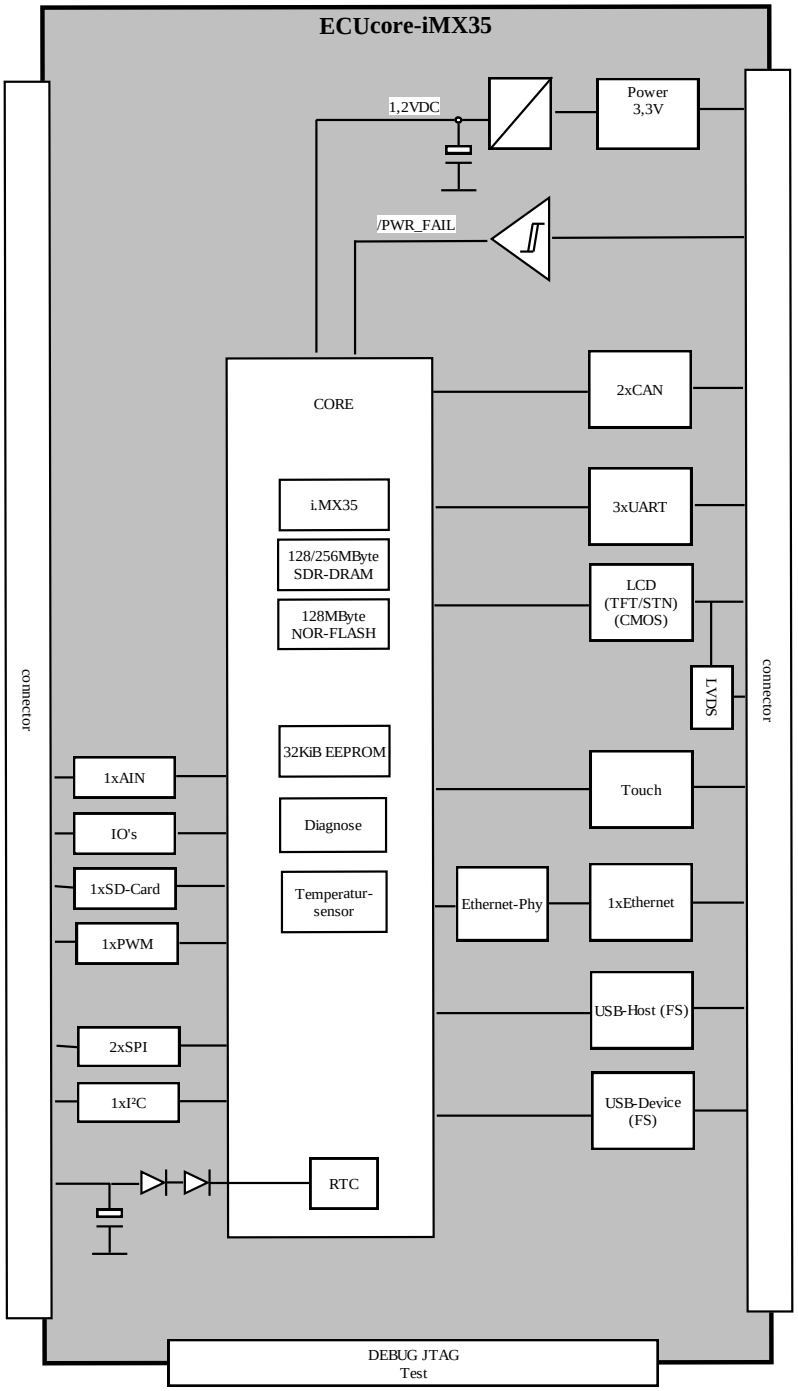

Figure 2: Block Diagram ECUcore-iMX35

4 Component Descriptions

The functions of the on-board components are explained in the following sections.

4.1 Connectors

The ECUcore-iMX35 has two board connectors. Each of the SMT socket strips consists of 100 contacts divided into double rows. In total the module has 200 contacts. For better EMC-properties, 20% of the pins are GND.
A third connector at the front side is for connecting debug interfaces of the CPU and the signal /DIS_NAND.

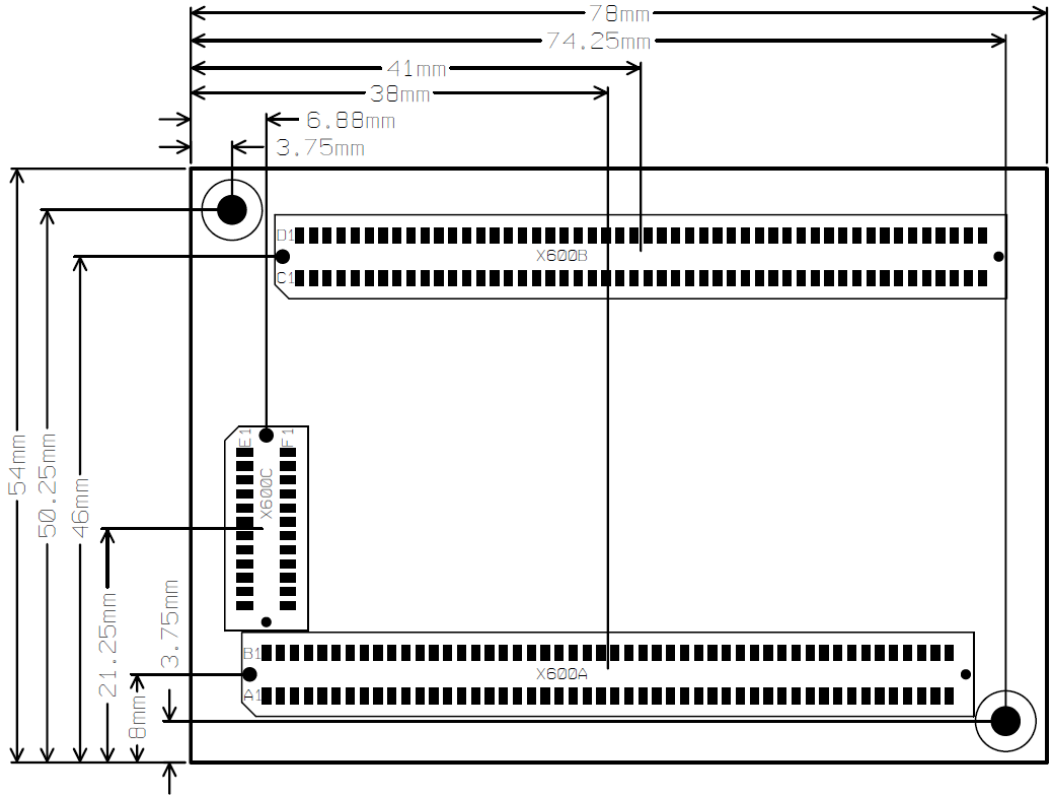

Figure 3: Pinout (top view)

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The picture shows the module from top view which means you look from the top through the module. The connectors are placed accordingly to the ones on the customer board.

The board connectors are equipped with the common and durable 1,27mm pitch. The type of socket stripes used on the ECUcore-iMX35 is '6060'-series provided by "W+P PRODUCTS" with a height of 3,6mm.

The series matches (e.g.) with "W+P PRODUCTS" strip line series '7072' or '7073'. Please refer to the datasheet and their electrical specifications.
Connectors:
ECUcore-iMX35:

W+P 6060-100-36-00-00-00-PPST (2x50pol. socked))
W+P 6060-024-36-00-00-00-PPST (2x12pol.)

Customer board:

W+P 7072-100-10-00-10-PPST (2x50pol. header)
W+P 7072-024-10-00-10-PPST (2x12pol.)

Table 1 and Table 2 define the pin out.

Signal	Pin	Pin	Signal
GND	A01	B01	GND
/BOOT	A02	B02	/MR
/BOOTSTRAP_1	A03	B03	/RESET
VSTBY	A04	B04	/PFI
/BOOTSTRAP_0	A05	B05	WDI
GND	A06	B06	/PFO
RXD1	A07	B07	GND
TXD1	A08	B08	RUN_STOP
RTS1	A09	B09	CTS2
CTS1	A10	B10	RTS3
GPIO2_12	A11	B11	5V_EN
GND	A12	B12	GND
TXD2	A13	B13	TXD3
RXD2	A14	B14	RXD3
NVCC_3V3	A15	B15	GPIO1_26
NVCC_3V3	A16	B16	GPIO2_18
GND	A17	B17	-
USBPHY2_DP	A18	B18	-
USBPHY2_DM	A19	B19	GND
USBPHY1_UID	A20	B20	USB_PHY1_DP

Signal	Pin	Pin	Signal
Unused	A21	B21	USB_PHY1_DM
GND	A22	B22	GND
I2C2_DAT	A23	B23	CAN1TX
I2C2_CLK	A24	B24	CAN1RX
GND	A25	B25	GPIO1_24
GPIO3_25	A26	B26	GND
GND3_26	A27	B27	/RESET
Unused	A28	B28	/PORESET
/EN_IO3V3	A29	B29	-
Unused	A30	B30	CAN2_RX
GND	A31	B31	CAN2_TX
CSPI1_SS0	A32	B32	GND
CSPI1_SS2/PWMO	A33	B33	/CS_ADC
CSPI1_MOSI	A34	B34	CSPI1_MISO
CSPI1_SS3	A35	B35	CSPI1_SCLK
Unused	A36	B36	-
GND	A37	B37	SD1_CK
SD1_CMD	A38	B38	GND
SD1_DATA0	A39	B39	SD1_DATA1
SD1_DATA2	A40	B40	SD1_DATA3
MATRIX_C1	A41	B41	MATRIX_C0
MATRIX_C3	A42	B42	MATRIX_C2
GND	A43	B43	MATRIX_R0
MATRIX_R1	A44	B44	GND
MATRIX_R3	A45	B45	MATRIX_R2
GPIO1_8	A46	B46	Run_LED
GPIO1_12	A47	B47	SD1_DET
VBAT	A48	B48	RS485_DEN
GND	A49	B49	GND
+3V3	A50	B50	+3V3

Table 1: Pin out connector X600A

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Signal	Pin	Pin	Signal
GND	C01	D01	+2V5_EPHY
ETH_TX-	C02	D02	GND
ETH_TX+	C03	D03	ETH_SPEED
ETH_RX+	C04	D04	ETH_LINK/ACT
ETH_RX-	C05	D05	GND
GND	C06	D06	GPIO1_6
GPIO1_0	C07	D07	GPIO1_5
GPIO1_1	C08	D08	GPIO1_4
GND	C09	D09	GND
PCB_V0	C10	D10	GPIO1_3
PCB_V1	C11	D11	/USBPHY2_OC
PCB_V2	C12	D12	/USBPHY2_PWR
PCB_V3	C13	D13	USBPHY1_VBUS
SD2_CLK	C14	D14	SD1_CMD
GND	C15	D15	GPIO1_31
LCD_VDD_ON	C16	D16	GND
-	C17	D17	SW_DIR
/TOUCH_INT	C18	D18	GPIO1_25
TOUCH_BUSY	C19	D19	SW_CLK
WD_TRIG	C20	D20	CLKO
GPIO2_15	C21	D21	MATRIX_INT
SW_S	C22	D22	USER_LED1
LCD_BL_VCC_ON	C23	D23	GND
GND	C24	D24	/LCD_BL_EN
5V_PG	C25	D25	USER_LED4
LCD_BL_PWM	C26	D26	USER_LED2
USER_LED3	C27	D27	USER_SW1
USER_SW2	C28	D28	GND
GND	C29	D29	USER_SW2
USER_SW4	C30	D30	-
LCD_TXout0+	C31	D31	LCD_TXout0-
LCD_TXout1+	C32	D32	LCD_TXout1-
LCD_TXout2+	C33	D33	GND
LCD_TXout2-	C34	D34	LCD_TXoutCLK+
GND	C35	D35	LCD_TXoutCLK-
LCD_R0	C36	D36	LCD_R1
LCD_R2	C37	D37	LCD_R3
LCD_R4	C38	D38	LCD_R5
LCD_G0	C39	D39	GND
LCD_G1	C40	D40	LCD_G2
GND	C41	D41	LCD_G3
LCD_G4	C42	D42	LCD_G5
LCD_B0	C43	D43	LCD_B1
LCD_B2	C44	D44	LCD_B3
LCD_B4	C45	D45	GND
LCD_B5	C46	D46	/LCD_BUS_EN
GND	C47	D47	/RESET_LCDCON
LCD_DEN	C48	D48	LCD_DCLK
LCD_HSYNC	C49	D49	LCD_VSYNC

Signal	Pin	Pin	Signal
GND	C50	D50	GND

Table 2: Pin out connector X600B

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Pin function:

Name	Function
/BOOT	for selecting software-boot-sequence going till uboot or linux image
/MR	manual reset input of module
/RESET	reset output signal of the voltage supervisor chip and of the CPU
/PFI	Power fail input for watching external power supply
WDI	watchdog input
BMS	boot mode select of CPU boot from NOR-Flash or SD-Card, …, USB
TXDx, RXDx, RTSx, CTSx, SCKx	USART 1,2,3 with handshake signals and clock signal (LV-TTL-level)
USBPHY2xx	USB-Host
USBPHY1xx	USB-Device
I2C2_DAT, I2C2_CLK	two wire interface
CANx_TX, CANx_RX	CAN 1,2 (LV-TTL-Level)
VBAT	backup battery input (3,3V) for RTC
ETH0_TX-, TX+, RX-, RX+; +2V5_EPHY	Ethernet-interface with reference voltage
GPIOx_xx	general purpose input / output pin
SDx_CMD, SDx_CLK, SDx_DATAx	SD-Card 1,2 interface pin
PWMO	Pulse width modulation output channel
CAPTURE, COMPARE	Timer Input/Output
+3V3	3,3V-supply (about 820mA)
GND	Signal ground

Table 3: Signal description connector X600A/X600B

The term in brackets (Table 1, Table 2) denotes the name of the Freescale iMX35 microcontroller port pins.

Note: All GPIO pins of iMX35 are capable to use as interrupt input.

Connector X600C:

Signal	Pin	Pin	Signal
+3V3	E1	F1	/RESET_IN
/JTAGSEL	E2	F2	GND
CPU_TDI	E3	F3	CPU_TDO
CPU_TCK	E4	F4	CPU_TMS
GND	E5	F5	CPU_TRSTB
CPU_RTCK	E6	F6	RXD1
TXD1	E7	F7	GND
PWR_TDI	E8	F8	PWR_TDO
PWR_TCK	E9	F9	PWR_TMS
GND	E10	F10	PWR_TDI
PWR_TDO	E11	F11	PWR_TCK
PWR_TMS	E12	F12	GND

Table 4: Pinout connector X600C

Pin function:
All pins are JTAG pins for debugging and programming the CPU.

4.2 Power Supply

The ECUcore-iMX35 must be supplied with an input voltage of +3.3VDC. The typical current consumption is approximately 820mA.

The 3,3V directly supplies:

- iMX35 IO voltage
- Flash, RAM, EEPROM
- RTC, Temperature sensor
- Ethernet PHY
- LCD controller

So be careful and provide a good voltage with low tolerance and low ripple. See "Technical Data" for detailed information.

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The on-board switching regulator generates all other needed voltages which is:

- 1,8V core voltage for iMX35
- 1,375V core voltage for iMX35
- 3,3V low drop core voltage for iMX35
- 1,5V low drop core voltage for iMX35

Reset Controller

Functions of the Reset Controller:

- watching 3,3V system voltage and reset the module if the voltage is too low
- monitoring power fail input from customer board
- manual reset input and stretched reset output
- 1,8sec watchdog timer

Watching voltage

Name	Voltage	Min Level
VCC_3V3	3,3V	3,1V
NVCC_3V3	3,3V	3,1V
NVCC_1V8	1,8V	1,7V
VDD_1V375	1,375V	1,347V
OVDD_3V3	3,3V	3,22V
PVDD_1V5	1,5V	1,42V

a) Watchdog

The Trigger-Pin 'WDI' is connected to the socket stripe X600A/B5. Any ECUcore-iMX35 pin can be connected externally to WDI.

b) Power fail

The power fail input of the Reset controller is connected to the socket stripe pin X600A/B04 with 10M pull-up to 3,3V. If the voltage at /PFI falls below 0,95V, the /PFO switches to low.

An external digital signal can be used to trigger a power fail interrupt. This can be the power good output (e.g. open collector output) of a power supply.

c) Manual Reset

The manual reset (/MR) is connected to X600A/B02 with 10k pull-up to 3,3V. A reset occurs if the manual reset is switched to GND.

If a reset occurs, /RESET_IN remains low for 53 ms. Reset out pin is connected to X600A/B03.

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4.3 Chip Configuration after Reset

The start vector depends on the Signals /BOOTSTRAP_0 (X600A/A5) and /BOOTSTRAP_1 (X600A/A2). If these pins are not connected, the default value 0b10 is set by pull-up/pull-down resistors.

Value of BOOTSTRAP[1:0] pins	Boot mode
0b00	Booting from internal ROM
0b10 (default)	Direct Boot from NOR Flash
0b11	Boot from UART or USB (Serial Download Boot Mode)

Table 5: Boot Modes

In case of "Serial Download Boot Mode" is selected the iMX35 determines the active serial port, either UART or USB, by polling the UART and USB status register for about 32 seconds. If there is no activity on either port within the predefined polling loop time,
then the ROM powers down the device using WDOG. In the USB/UART bootloader valid case, the WDOG is serviced periodically. If the communication between the iMX35 and boot device hangs for more than 32 sec or the processor goes into an endless loop, then WDOG expires and powers down the device.

iMX35 starts with a start-up configuration with fixed bus width, bus frequency, timing and control signals. Changes are not possible via configuration pins.

4.4 SDRAM

The iMX35 has two external bus interfaces up to 32bit de-multiplexed. The first interface is shared by SDRAM and NOR-Flash.

Two 16bit-Synchronous DRAMs are mounted and connected as one RAM with 32bit-buswidth.
The RAM density is 2x64MiB.

By default, a RAM with 7,5ns cycle time for 133MHz bus frequency is mounted. It supports the PC133 bus mode of CPU.

4.5 NOR-Flash

The board is equipped with NOR-Flash because it provides a higher security in terms of data retention compared to NAND-Flash. NAND-Flash works with bad sectors can be problematic if such sector influences the boot-up routine of the module in early time. The module is designed for industrial applications with high requirements for safe operation.

The Flash (default: 1x Micron PC28F00AM29EWHA) is connected via a 16bit bus. It works with 25ns access time. The density is 128MiB.

4.6 Ethernet Controller

The iMX35 supports one 10/100MBit/s Ethernet channel by an internal MAC with MII/RMII interface.
An on-board PHY chip KS8721BLI from Micrel allows for a 10/100 MBit/s physical interface. The PHY is connected with the RMII interface of the CPU.

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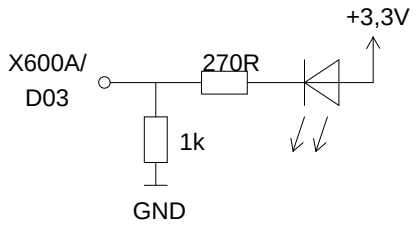
Board connector signals are:

Signal	Description
ETH_TX+	Tx+ from PHY
ETH_TX-	Tx- from PHY
ETH_RX+	Rx+ from PHY
ETH_RX-	Rx- from PHY
2V5_EPHY	2,5V PHY-Supply as reference for transformer
ETH_LINK/ACT	output of PHY-LED0 low-active
ETH_SPEED	output of PHY-LED1 low-active

Table 6: Ethernet signals

Note: Connect ETH_LINK/ACT and ETH_SPEED LED with a 270R series resistor, not directly!

The ETH_SPEED LED is also a strapping pin, which means that this pin is read at reset. When the pin is open (or high with LED), the PHY is configured for 100MBbps speed. If you need forced 10MBbps, place a 1k pull-down resistor to GND at this pin.



Tx and Rx Signals are pulled up with 49,9R to 2,5V-EPHY on-board. So you need only the transformer and connector as external components for communication.

SYS TEC electronic has acquired a pool of these MAC addresses. The MAC address for the first Ethernet interface Eth0 is barcode-labelled and attached on the ECUcore-iMX35.

4.7 I2C Module

The ECUcore-iMX35 features one I2C interface. This is a 2-wire serial bus used for communication with I2C devices. The bus is brought out via the board connector. The ECUcore-iMX35 comes with two on-board I2C devices. Please refer to the table below.

I2C device	Address
Real-Time-Clock Epson 8564JE (U2)	0x51
Temperature Sensor TI TMP101 (U3)	0x49 with R_ADD0 open (default) 0x48 with R_ADD0 4k7 (R10)

Table 7: I2C Components

4.7.1 Real Time Clock

The ECUcore-iMX35 is equipped with a Real time clock to manage real-time applications. The device offers functions such as calendar clock, alarm and timer. It also outputs pre-defined frequencies (32.768kHz, 1024Hz, 32Hz, 1Hz) via the CLKOUT pin.

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RTC characteristics:

- Built-in crystal running at 32768Hz
- Programmable alarm, timer and interrupt functions
- Low power consumption:

    - Bus active: ≤ 1mA
    - Bus inactive, CLKOUT inactive: ≤ 1µA

The Real time clock is supplied with 3.3V DC. If the system voltage is off, a backup battery or cap (connected at X600/A48) supplies the RTC. This battery or cap must be placed on the customer board.

Device address:

- 0xA2 when write mode
- 0xA3 when read mode

The pin CLKOE is connected to 3.3V DC. So the clock output can be enabled by setting the bit 'FE' in register 'Clock Out frequency' to 1.

CLKOUT and RTC_INT are connected to iMX35 to be used by the application.

Signal	**Pin at iMX35**
CLKOUT	MLB_SIG / GPIO3_5
/RTC_INT	MLB_CLK / GPIO3_3

4.7.2 Temperature Sensor

The ECUcore-iMX35 features a Temperature sensor TMP101 to record ambient temperatures to, e.g., enable protection from overheating. The ECUcore-iMX35 just provides the physical connection between the CPU and the sensor. The communication or any protective measures are software functions to be provided by the user application.

The address is adjustable by a resistor. The following table shows the various assembly options.

Resistor	ADD0 signal	Address
R10 equipped (default)	0 (GND)	1001000x = 0x90
R10 open	floated	1001001x = 0x91

Table 8: Temperature Sensor Address

Temperature sensor characteristics:

- Temperature resolution of 0.0625°C
- Temperature range of -55°C to +125°C
- Alert pin as interrupt source if temperature exceeds defined limits

The Alert-Pin is connected to iMX35 to be used by the application (Pin Y13 (GPIO3_4)).

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4.8 SPI Module

The ECUcore-iMX35 allows high-speed serial communication with SPI devices such as EEPROM via two SPI interfaces. The SPI interfaces contain four chip select (CS) signals each. The SPI bus signals are directly dumped via the board connector.

There is one EEPROM connected to the SPI on-board. The on-board EEPROM is connected to CSPI2 and occupy CSPI2_SS0.

The following table shows the available SPI signals.

X600-Pin	Connector signal	SPI signal	Description
A32, B33, A33 A35	CSPI1_SS0 CSPI1_SS1 CSPI1_SS2/PWMO CSPI1_SS3	/CSPI1_SS0 /CSPI1_SS1 /CSPI1_SS2 /CSPI1_SS3	SPI-Chip Select
A34	CSPI1_MOSI	CSPI1_MTSR (SOUT)	Master Transmit Slave Receive
B34	CSPI1_MISO	CSPI1_MRST (SIN)	Master Receive Slave Transmit
B35	CSPI1_SCCK	SPI_CLK (SCK)	Clock

Table 9: SPI Signals

4.8.1 On-board EEPROM

The ECUcore-iMX35 is equipped with one on-board EEPROM. The EEPROM (default AT25256AN 32KiB) can be used to store user data and/or configuration data. It is connected to the iMX35 via SPI module CSPI2. The EEPROM uses chip select SS0 CSPI2.

The EEPORM supports SPI Modes 1 and 3. There is no separate erase cycle needed before writing.

4.9 Display Support

To simplify the development of devices that require human machine interfaces, the ECUcore-iMX35 supports interfacing LCD and TFT displays directly. The ECUcore-iMX35 always includes an LCD controller.

Optionally the ECUcore-iMX35 can be equipped with an LVDS controller to support longer distances between the ECUcore-iMX35 board and the connected display.

4.9.1 LCD Controller

The iMX35 features an on-chip LCD controller. It consists of the logic transferring LCD image data from an external display buffer to an LCD module with integrated common and segment drives.

The LCD controller supports single and double scan monochrome and color passive STN LCD modules. It also supports single scan active TFT LCD modules. Resolutions up to 800x600 pixels can be driven. The maximum pixel depth without any restrictions is 24bits (8bits per color channel).

The ECUcore-iMX35 is designed to use a maximum pixel depth of 24bits. The following table shows the signals that are dumped out of the board via X600

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X600-Pin	Connector signal	Description
C36, D36, C37, D37, C38, D38	LCDx_Rx	LCD data bus output (red)
C39, C40, D40, D41, C42, D42	LCDx_Gx	LCD data bus output (green)
C43, D43, C44, D44, C45, C46	LCDx_Bx	LCD data bus output (blue)
D47	/RESET_LCD_CON	LCD reset signal
C48	LCD_DEN	Data enable signal
D48	LCD_DCLK	LCD clock signal (STN/TFT)
C49	LCD_HSYNC	Line synchronous signal (STN) or Horizontal synchronous signal (TFT)
D49	LCD_VSYNC	Frame synchronous signal (STN) or Vertical synchronization signal (TFT)

Table 10: LCD controller signals

The pins can be connected directly to an appropriate passive STN LCD or active TFT LCD module.

4.9.2 LVDS Controller

Upon request the ECUcore-iMX35 can be equipped with an LVDS controller (DS90C365AMT from National). The LVDS controller is useful, if the display has to be connected by longer wires to the ECUcore-iMX35 or if there are higher requirements for disturbance resistance. The following table shows the available signals of the LVDS controller.

X800-Pin	Connector signal	LVDS controller signal
C31	LCD_TXout0+	TXOUT0+
D31	LCD_TXout0-	TXOUT0-
C32	LCD_TXout1+	TXOUT1+
D32	LCD_TXout1-	TXOUT1-
C33	LCD_TXout2+	TXOUT2+
C34	LCD_TXout2-	TXOUT2-
D34	LCD_TXoutCLK+	TxCLK OUT+
D35	LCD_TXoutCLK-	TxCLK OUT-
D46	/LVDS_PWD	PWDN

Table 11: LVDS controller signals

The power down signal /LVDS_PWD of the LVDS controller is pulled up by 10k on-board. To enter power down mode of the LVDS controller the /LVDS_PWD signal can be pulled low by externally connecting any general purpose output pin to that signal.

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4.10 CAN Interface

The ECUcore-iMX35 includes two CAN interfaces. It is realized by the on-chip CAN controller of the iMX35. The CAN bus is brought out via the board connector as LVTTL interface.

Externally a 3,3V CAN transceiver can be directly connected to CAN. Alternatively, a galvanic decoupled CAN interface can be built to save the module for high voltage transients.

4.11 Serial Interface

The iMX35 supports up to 3 independent USARTs. They feature individual baud rate generators, IrDA® infrared modulation / demodulation, hardware handshaking and DMA transerfs.

All USARTs are available on the board connector with the following lines: RXD, TXD, CTS, RTS and SCK.

All signals are brought out with LVTTL-Level. They are used to interface serial communication via RS232, RS422 or RS485 by external transceivers.

4.12 SDCard/MMC Interface

The ECUcore-iMX35 supports two multimedia-card interfaces. Both MMC interfaces (MCI1 – slot A and MCI0 –slot B) are brought out via connector. Each interface has 4 data pins for the usage as SD-Card or MMC interface.

Card Detect and Card Protect are not supported by default on ECUcore-iMX35 pin connector. Use general purpose IO Pins to watch these signals. MicroSD-card sockets only provide SLOT-contact to indicate a closed socket.

4.13 USB Interfaces

The iMX35 provides one USB2.0 (480Mbit/s) device and one USB2.0 (480Mbit/s) host interfaces. Each interface is brought out at the connector with its P and M signal.
No security components (such as TVS-Diodes) are provided at the module, they have to be mounted near the USB connector on the customer board.
Over-current protection is not supported by default. If necessary, use an external current limiting device with over-current-flag and connect it to one of the iMX35 general purpose IOs.

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4.14 Embedded ICE Port

The Embedded ICE-Port is not provided by the series module. It requires the socket stripe X600C. This connector is not mounted.

ECUcore-iMX35 is supposed for programming in Linux. There is no hardware debugging needed at all. For a Debug at this interface, a separate Debugger is needed as well.

Through the mounting process and while using the connector, the ARM_x signals are relevant for ICE and have to be connected to the debugger. No pull-up or pull-down resistors are required. A pull-up resistor of 10k are mounted on-board at /RESET_IN, TDI, TMS and TCK.

The /JTAGSEL pin is for selecting the ICE or JTAG mode. The JTAG mode is for the usage with Boundary Scan hardware and not needed for debugging. So leave open the pin when using ICE! For using JTAG, put it to GND.

5 Technical Data

The physical dimension of the ECUcore-iMX35 is shown in the figure below.

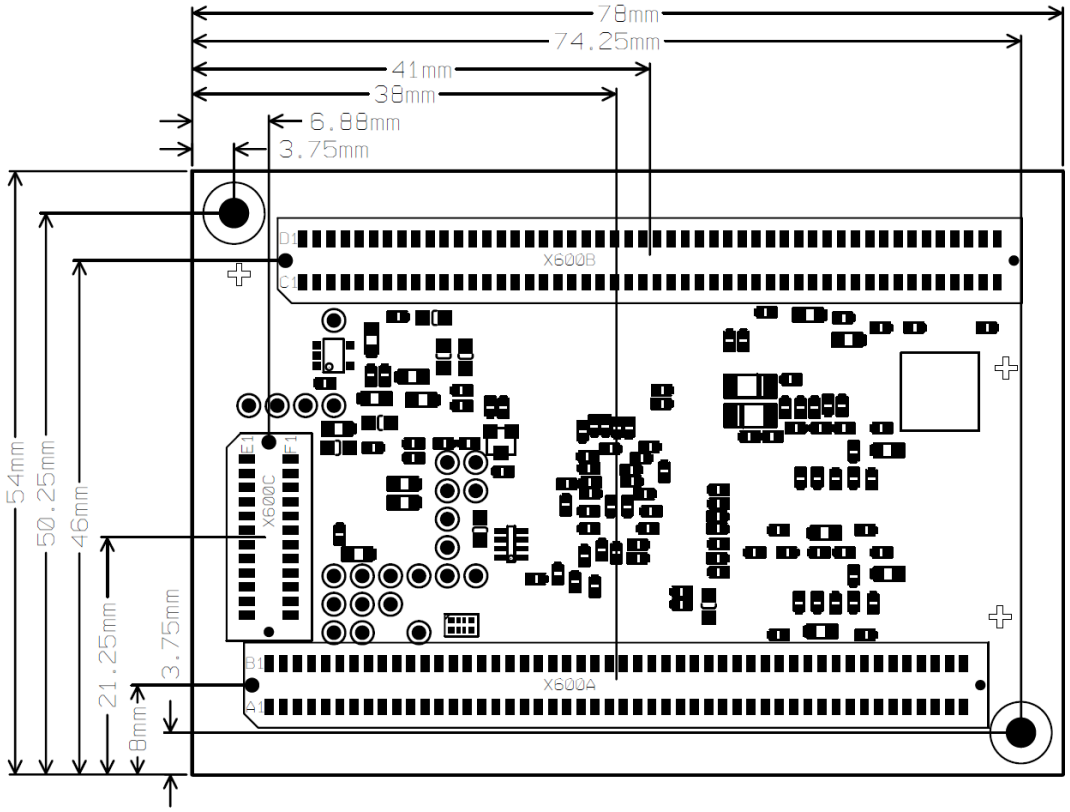

Figure 4: Physical Dimensions

The height including the board connector and components is about 8mm. The thickness of the PCB is about 1.6mm. The maximum component height on top is about 3mm.

dimensions	78mm x 54mm x 8mm
weight	approximately 21,5g
operating temperature	-40°C to +85°C
storage temperature	-40°C to +85°C
operating voltage	3.3V DC ± 5%
current consumption	typ. 820mA
I/O-Level	3.3V DC ± 5%

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Table 12: Technical Data

Document:	Hardware Manual ECUcore-iMX35
Document number:	L-1570e_01, Edition July 2014

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Did you find any mistakes in this manual? page

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